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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,111	03/10/2004	Dean A. Klein	M4065.0959/P959	2460

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

EXAMINER	
LUU, MINER PHO	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,111	KLEIN A. DEAN	
	Examiner	Art Unit	
	Pho M. Luu	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *Amendment filed on 08/04/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-61,69-73 and 81-85* is/are allowed.

6)☒ Claim(s) *1-8,62-65 and 74-77* is/are rejected.

7)☒ Claim(s) *9-11,66-68 and 78-80* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/04/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

1. Acknowledgment is made of applicant's Amendment filed 04 August 2005. The changes and remarks disclosed therein were considered.

2. Claims 1-85 are pending in the application.

Information Disclosure Statement

3. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 04 August 2005. The information disclosed therein was considered.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-4, 5, 7-8, 62, 64-65, 74 and 76-77 are rejected under 35 U.S.C. 102(e) as being anticipated by Burgan. (US. 6,778,457).

Regarding claims 1 and 3-4, Burgan in Figure 1 disclosed a memory refresh circuit (10) comprising:

a control circuit (control circuit 14 used to accessing the memory array for read, write and refresh operation with a plurality of conductor in memory 10, see column 2, lines 51-54) for conducting a memory refresh operation (refresh control circuit 16 control and coordinated refresh operation of memory 12 in response to control circuit 14, see column 3, lines 3-13) for monitoring a memory device (monitor circuit 18) and for indicating when the refresh operation is complete based on the monitoring (refresh control 16 receive refresh request output from monitor circuit 18 which is receive a plurality of signals PASS/FAIL-1 to PASS/FAIL-4) of the memory device (see column 3, lines 14-20).

Regarding claims 5 and 7-8, Burgan in Figure 1 disclosed a memory device (10) comprising:

a memory array (12);

a refresh circuit (control circuit 14 used to accessing the memory array for read, write and refresh operation with a plurality of conductor in memory 10, see column 2, lines 51-54) for controlling a refresh operation (refresh control circuit 16 control and coordinated refresh operation of memory 12 in response to control circuit 14, see column 3, lines 3-13) of the memory array (12) for monitoring a memory array (monitor circuit 18) and for indicating when the refresh operation is complete based on the monitoring (refresh control 16 receive refresh request output from monitor circuit 18 which is receive a plurality of signals PASS/FAIL-1 to PASS/FAIL-4) of the memory array (see column 3, lines 14-20).

Regarding claims 62 and 64-65, Burgan in Figure 1 disclosed an integrated circuit comprising:

memory device (10) comprising:

a memory array (12);

a refresh circuit (control circuit 14 used to accessing the memory array for read, write and refresh operation with a plurality of conductor in memory 10, see column 2, lines 51-54) for controlling a refresh operation (refresh control circuit 16 control and coordinated refresh operation of memory 12 in response to control circuit 14, see column 3, lines 3-13) of the memory array (12) for monitoring a memory array (monitor circuit 18) and for indicating when the refresh operation is complete based on the monitoring (refresh control 16 receive refresh request output from monitor circuit 18 which is receive a plurality of signals PASS/FAIL-1 to PASS/FAIL-4) of the memory array (see column 3, lines 14-20).

Regarding claims 74 and 76-77, Burgan in Figure 1 disclosed a processor system comprising a processor and a memory device (10):

a memory array (12);

a refresh circuit (control circuit 14 used to accessing the memory array for read, write and refresh operation with a plurality of conductor in memory 10, see column 2, lines 51-54) for controlling a refresh operation (refresh control circuit 16 control and coordinated refresh operation of memory 12 in response to control circuit 14, see column 3, lines 3-13) of the memory array (12) for monitoring a memory array (monitor

circuit 18) and for indicating when the refresh operation is complete based on the monitoring (refresh control 16 receive refresh request output from monitor circuit 18 which is receive a plurality of signals PASS/FAIL-1 to PASS/FAIL-4) of the memory array (see column 3, lines 14-20).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 6, 63 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burgan. (US. 6,778,457) in view of Jakobs et al. (US. 6,909,657).

Regarding to dependent claim 2, 6, 63 and 75, Burgan teaches a memory refresh circuit having all the basic limitations of the claimed invention, and further including the refresh circuit (16). However, Burgan fails to explicitly mention the refresh circuit including a refresh counter in a memory device.

Jakobs et al, for example, discloses a refresh counter (8, Fig. 1).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the memory device of Burgan with the aforementioned teaching of Jakobs et al. for the purpose of incremented the refresh request signal in order to generate the refresh signal depending on the counter reading of the refresh request counter (see column 3, lines 48-52).

10.17.05

Allowable Subject Matter

8. Claims 9-11, 66-68 and 78-80 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, 66 and 78, the prior art of record do not disclose or suggest a memory device including the control logic circuit providing a first control signal to the refresh circuit and second control signal to the control logic circuit.

9. Claims 12-61, 69-73 and 81-85 are allowed.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to: "a combining circuit for combining the refresh completed signals from the memory device to obtain a combined refresh complete signal" as claimed in the independent claim 12 and independent claim 24; or

"a temperature integration circuit for incorporating temperature into a refresh operation" as claimed in the independent claim 35 and independent claim 42; or

"a refresh circuitry is adapted to initiate the refresh operation partially in response to the environmental condition sense by the sensor which is indicate when the refresh operation is complete" as claimed in the independent claim 45, independent claim 69 and independent claim 81.

"a refresh completed signal when the burst self-refresh operation has been completed" as claimed in the independent claim 50; or

"a refresh complete signal form each memory device in the subset when the memory device complete the refresh operation" as claimed in the independent claim 61.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Pho M. Luu whose telephone number is 571.272.1876. The examiner can normally be reached on M-F 8:00AM – 5:00PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Richard Elms, can be reached on 571.272.1869. The official fax number for the organization where this application or proceeding is assigned is 703.872.9306 for all official communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PML
October 16 2005

10-17-05
RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800